IN THE DRAWINGS

Enter changes to add additional details and numerals shown in Figure 1 and Figure 2 attached.

IN THE SPECIFICATION

Amend paragraphs [19], [26] and [29] as follows:

[0019] Voltage isolation enables independent voltage levels to be supplied to logic and memory segments during test. Memory and logic test often require different voltage levels during respective testing. Voltage isolation may be achieved in several ways: (a) separate Vdd planes (84) (i.e. off-chip), (b) voltage regulators (82) that generate each macro voltage level from an external reference voltage, (c) a control feature in the BIST (81) engine that controls a reference to the voltage regulator for each macro, or (d) feedback (83) from the logic portion of the chip to the regulator to control voltage levels. It should be understood that other well known techniques exist in the field that could also be used in this system to provide voltage isolation such that the invention should not be limited to the examples listed above.

[26] A built in self test system, circuits not shown; generate the test signals for the memory macro portion 23. Circuits 30 (clocking isolation elements) disable the test clocks to the memory macro(s) during BIST testing so that the "Clock Mult & Control" circuit 11 block can generate BIST test clocks based on the reference frequency input

from the tester, (or alternatively from the OPCG ckt (25). The control circuit 11 also generates the control signal to the ~~multiplor~~ multiplexer 35 which selects the test clocks generated by the "Clock Mult & Control" block during the operation of the BIST. This enables independent test clocks to be applied to the memory and logic segments. During scan operations, the clocks enable the global test clocks so that BIST contents can be properly unloaded (scanned out) as described hereinafter.

[29] Scan bypass enables isolation of memory macros from the scan chains. This isolation is necessary during parallel test in order to load logic test patterns and unload test results via scan chains while the BIST engine is running. Figure 2 illustrates the preferred embodiment for scan bypass/isolation. Either a primary input 40 or general purpose test register latch 40 may be used to provide a control signal (labeled "bypass") to a multiplexer ~~30~~ 50 (scan chain bypass isolation element) in each memory segment. The scan chain is used to load the BIST pattern. Once the BIST operation pattern is loaded from input 42, the control signal from the test latch 40 puts the MUX 30 into bypass mode by selecting the scan in signal, not the output 44 of the BIST engine. Logic patterns can then be loaded and results unloaded via the scan chains while the BIST engine is running. When the BIST is done, the bypass mux is taken out of the bypass mode and the results can be unloaded via the scan chains using the clocking scheme described earlier.